



# DCR4100W42

# **Phase Control Thyristor**

DS5753-5 February 2014 (LN31294)

## **FEATURES**

- Double Side Cooling
- High Surge Capability

## **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

## **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR4100W42 DCR4100W40 DCR4100W35 DCR4100W30	4200 4000 3500 3000	$\begin{split} &T_{vj} = \text{-}40^{\circ}\text{C to 125}^{\circ}\text{C}, \\ &I_{DRM} = I_{RRM} = 200\text{mA}, \\ &V_{DRM}, V_{RRM}  t_p = 10\text{ms}, \\ &V_{DSM}  \&  V_{RSM} = \\ &V_{DRM}  \&  V_{RRM} + 100V \\ &\text{respectively} \end{split}$

Lower voltage grades available.

# **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

## DCR4100W42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### **KEY PARAMETERS**

$V_{DRM}$	4200V
$I_{T(AV)}$	3880A
I <sub>TSM</sub>	53500A
dV/dt*	1500V/µs
dl/dt	400A/μs

# \* Higher dV/dt selections available

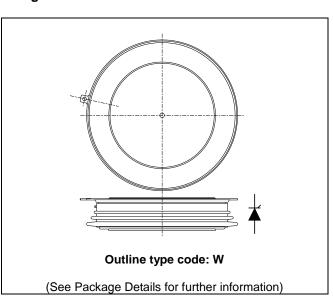


Fig. 1 Package outline



# **CURRENT RATINGS**

# $T_{case} = 60$ °C unless stated otherwise

Symbol	Parameter	Test Conditions		Units
Double Sid	de Cooled			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	3880	А
I <sub>T(RMS)</sub>	RMS value	-	6095	А
I <sub>T</sub>	Continuous (direct) on-state current	-	5725	А

# **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	53.5	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 0$	14.31	MA <sup>2</sup> s

# THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Condition	Min.	Max.	Units	
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	Double side cooled DC		0.00631	°C/W
		Single side cooled	Anode DC	-	0.01115	°C/W
			Cathode DC	-	0.01453	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 76kN	Double side	-	0.0014	°C/W
		(with mounting compound)	Single side	-	0.0028	°C/W
T <sub>vj</sub>	Virtual junction temperature	Blocking V <sub>DRM</sub> / <sub>VRRM</sub>		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
F <sub>m</sub>	Clamping force			68.0	84.0	kN





# **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditio	ns	Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125$ °C, ga	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub>	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	400	A/µs
		$t_r < 0.5 \mu s, T_j = 125 ^{\circ} C$				
V <sub>T(TO)</sub>	Threshold voltage – Low level	700A to 4100A at T <sub>case</sub> = 125	5°C	-	0.83	V
	Threshold voltage – High level	4100A to 12000A at T <sub>case</sub> = 125°C		-	1.0	V
r <sub>T</sub>	On-state slope resistance – Low level	700A to 4100A at T <sub>case</sub> = 125°C		-	0.1688	mΩ
	On-state slope resistance – High level	4100A to 12000A at T <sub>case</sub> = 125°C		-	0.1263	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, $10\Omega$		TBD	TBD	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$T_j = 125$ °C, $V_R = 200$ V, $dI/dt = 100$	= 1A/µs,	250	500	μs
		dV <sub>DR</sub> /dt = 20V/μs linear				
Qs	Stored charge	$I_T = 2000A$ , $T_j = 125$ °C, $dI/dt - 1A/\mu s$ ,		1500	4500	μC
ΙL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	А
I <sub>H</sub>	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500$	0A, I <sub>T</sub> = 5A	-	300	mA





# **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	$V_{DRM} = 5V$ , $T_{case} = 25$ °C	1.5	V
$V_{GD}$	Gate non-trigger voltage	At V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	$V_{DRM} = 5V$ , $T_{case} = 25$ °C	350	mA
I <sub>GD</sub>	Gate non-trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	10	mA

## **CURVES**

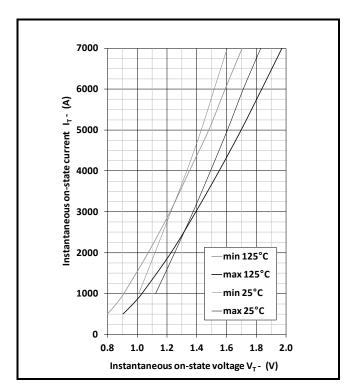


Fig.2 Maximum & minimum on-state characteristics

 $V_{\text{TM}}$  EQUATION

Where A = 0.348967

B = 0.066851C = 0.000102

D = 0.003788

 $V_{TM} = A + BIn (I_T) + C.I_T + D.\sqrt{I_T}$ 

these values are valid for  $T_j = 125$ °C for  $I_T 500$ A to 10000A

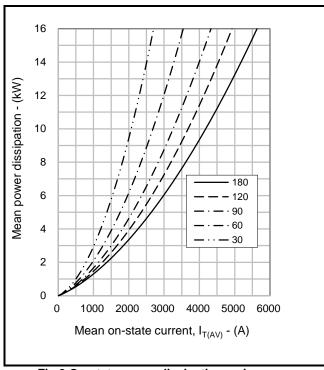


Fig.3 On-state power dissipation - sine wave

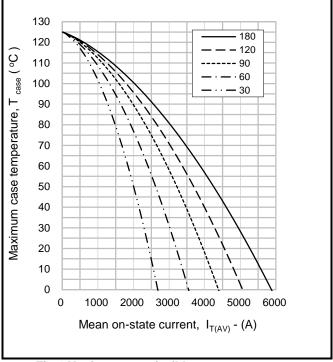


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

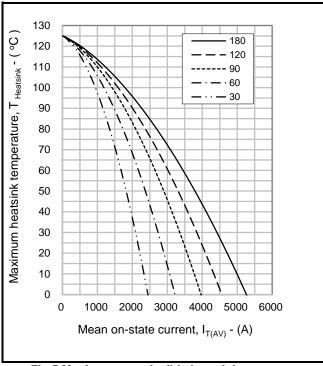


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

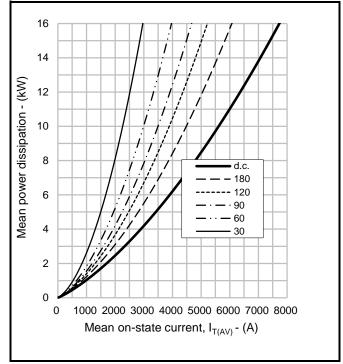
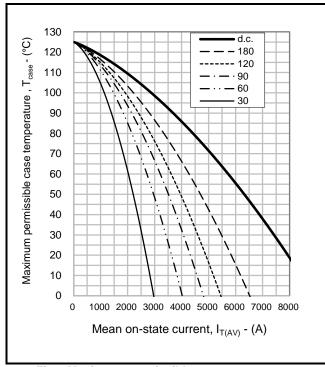
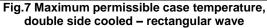


Fig.6 On-state power dissipation - rectangular wave





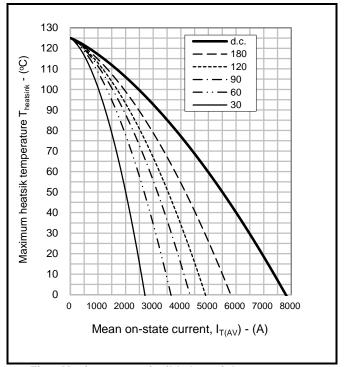
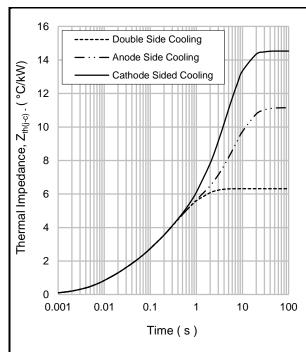


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	0.8816	1.2993	2.8048	1.3305
	T <sub>i</sub> (s)	0.0106818	0.058404	0.3584979	1.1285
Anode side cooled	R <sub>i</sub> (°C/kW)	1.5197	3.2398	5.7622	0.6312
	T <sub>i</sub> (s)	0.0170581	0.2424644	6.013	15.364
Cathode side cooled	R <sub>i</sub> (°C/kW)	1.4106	2.4667	6.7451	3.9054
	T <sub>i</sub> (s)	0.0158344	0.1786951	3.6201	6.196

 $Z_{th} = \sum [R_i x (1-exp. (t/t_i))]$  [1]

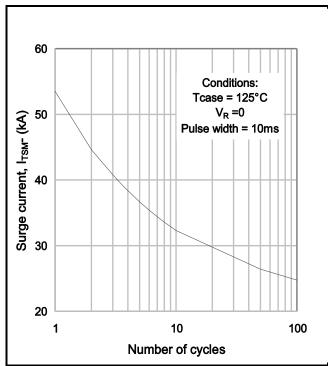
 $\Delta R_{\text{th(j-c)}}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

Double side cooling					Anode Side	Coc
	$\Delta Z_{th}$ (	$\Delta Z_{th}(z)$			$\Delta Z_t$	h (2
θ°	sine.	rect.		θ°	sine.	
180	1.00	0.67		180	0.94	
120	1.16	0.97		120	1.08	
90	1.33	1.13		90	1.23	
60	1.48	1.31		60	1.37	
30	1.61	1.51		30	1.47	
15	1.66	1.61		15	1.52	

Cooling	l	Cathode Sided Cooling			
(z)			$\Delta Z_{th}$ (z)		
rect.		θ°	sine.	rect.	
0.64	l	180	0.95	0.65	
0.91		120	1.09	0.92	
1.06	[	90	1.25	1.07	
1.22		60	1.38	1.23	
1.38	[	30	1.49	1.40	
1 17	ĺ	15	1 5 1	1.40	

Fig.9 Maximum (limit) transient thermal impedance - junction to case (°C/kW)





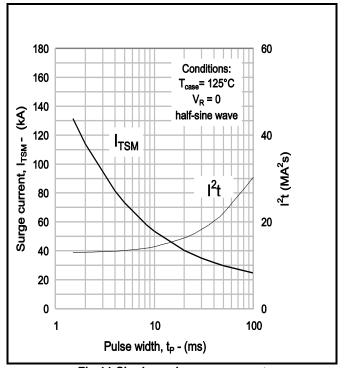


Fig.11 Single-cycle surge current

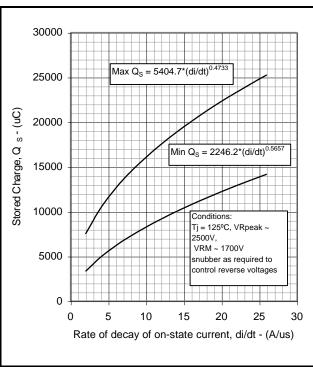


Fig.12 Stored charge

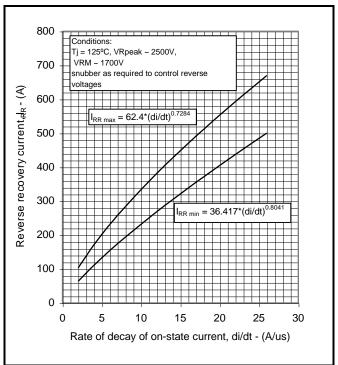


Fig.13 Reverse recovery current

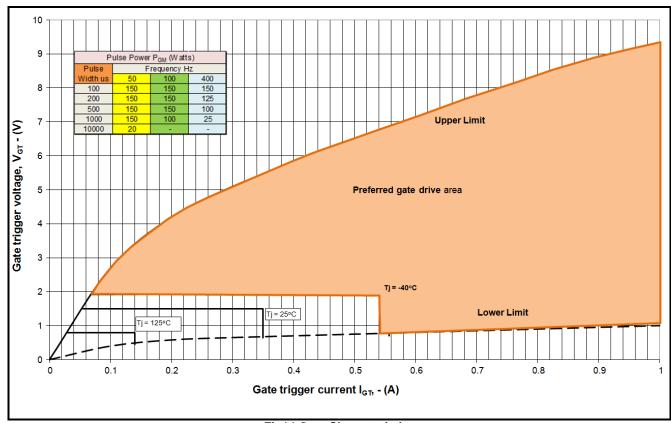


Fig14 Gate Characteristics

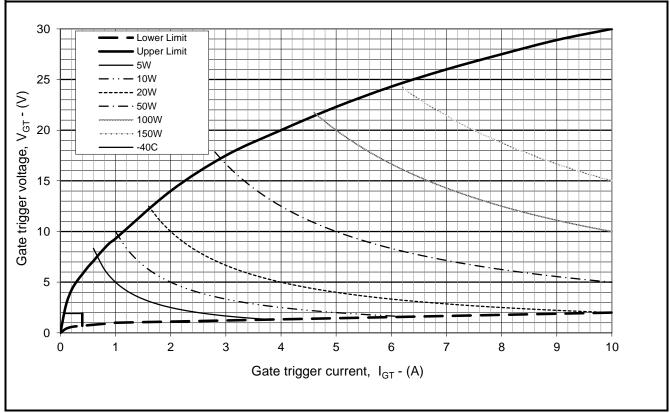


Fig. 15 Gate characteristics





### PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

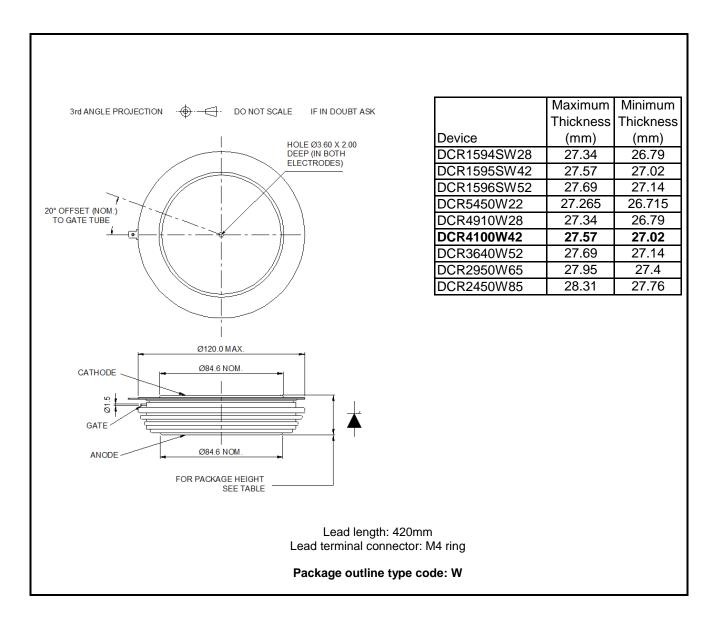


Fig.16 Package outline





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